REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific issues raised in the present Office Action, applicants acknowledge, with thanks, the Examiner's indication that Claims 13, 25 and 29 would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Despite the indication of allowable subject matter, applicants have not amended the claims to include the allowable subject matter since broader coverage is available. Applicants, however, reserve their right to amend the claims to include the allowable features of Claims 13, 25 and 29 at a later date, if needed.

Applicants have amended Claims 1-5, 12, 14-16, and 20-22 by changing the phrase "SOI structure" to "SOI substrate". Support for this amendment to each of the aforementioned claims is found throughout the entire specification of the instant application. See, for example, paragraphs [0021], [0022], [0023] and [0045].

Since the above amendments to the claims do not introduce new matter into the instant application, entry thereof is respectfully requested.

In the present Office Action, the drawings are objected to under 37 C.F.R. § 1.83(a) as allegedly not showing a BiCMOS element. Applicants respectfully disagree with the Examiner and note that it is well known to those skilled in the art that a BiCMOS device is an integrated bipolar transistor and a CMOS transistor. See, for example, paragraphs [0003] and [0009] of the specification of the instant application in which the term "BiCMOS" is defined. Applicants submit that this definition of BiCMOS is consistent with that found in U.S. Patent No. 5,620,908 to Inoh, et al. ("Inoh, et al.),

which reference was applied against the claims of the present application, as allegedly rendering the same obvious. Applicants make reference to the formal drawings that were submitted to the USPTO on April 28, 2004, especially FIG. 2 and FIG. 3M in which a CMOS transistor, i.e., FET 112, is present in the CMOS device region 102, and the bipolar device of the BiCMOS device, which is represented by emitter region 50 and base region 42m, is present in the BiCMOS device region 100. Applicants respectfully submit that the drawings do indeed show the alleged missing BiCMOS element therein. Thus, no corrections to the drawings are needed.

In view of the above remarks, the objection to the drawings under 37 C.F.R. § 1.83(a) can and should be withdrawn. Reconsideration and withdrawal of the instant drawing objection are thus respectfully requested.

Claims 1-12, 14-24, and 26-28 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the disclosure of Inoh, et al.

Applicants respectfully submit that the claims of the present application are not rendered unpatentable by the disclosure of Inoh, et al. Specifically, applicants observe that in Inoh, et al. the substrate 100 is a bulk Si wafer, not a SOI wafer which includes an SOI layer, a buried insulating layer and a bulk semiconductor layer. The SOI layer of a SOI substrate is generally the area in which at least one active device such as a CMOS is formed. See FIG. 2 of the present invention. SOI substrates provide high-speed IC's over their bulk counterparts. Moreover, the SOI substrates provide higher performance, absence of latch-up, higher packing density and low voltage applications than a bulk substrate. One problem of using SOI substrates which is avoided by the present invention, is the topographic issue. In the present invention, the use of the SOI substrate permits the HBT to built on the upper surface of the semiconductor substrate of the SOI

substrate, while the CMOS transistor is built on the SOI layer. Thus, the CMOS transistor has SOI properties, while the bipolar transistor has bulk like properties.

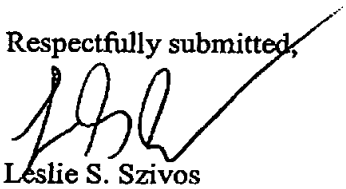
Applicants observe that in Inoh, et al. reliance is made on elements 100, 108 and 110 as forming an SOI substrate. This is not correct. Layer 108 is an insulating interlayer that is formed over the entire surface of a bulk substrate 100 after CMOS devices are formed. Layer 110 is silicon oxide. Thus, the structure disclosed in the applied reference comprises a bulk semiconductor substrate 100 having an insulating stack comprised of layers 108 and 110. This is different from a SOI substrate which as known to those skilled in the art includes a buried insulating layer separating two semiconductor layers. Applicants observe that the various materials mentioned in paragraph [0045] of the present application for the top Si-containing layer are all materials that are semiconducting.

The §103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed structures and methods to include the various features recited in the claims of the present invention. In particular, Inoh, et al., do not teach or suggest the possibility of replacing a bulk substrate with an SOI substrate. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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